REMARKS

This communication is in response to the Office Action dated December 17, 2002. Claims 1,2 and 4-18 are pending in the present Application. Claims 17 and 18 have been objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims. Claims 1,2 and 4-18 have been canceled. Claims 19- 21 have been added and include the allowed subject matter. Claims 1, 2 and 4-21 remain pending in the present Application.

Attached hereto is a marked-up version of the changes made to the claims by the current amendment. The attached pages are captioned "Version with markings to show changes made."

Applicant believes that this application is in condition for allowance. Accordingly, Applicant respectfully requests reconsideration, allowance and passage to issue of the claims as now presented. Should any unresolved issues remain, Examiner is invited to call Applicant's attorney at the telephone number indicated below.

Respectfully submitted,

Wendell J. Jones
Attorney for Applicant
Reg. No. 45,961
(408) 938-0980

VERSIONS WITH MARKINGS TO SHOW CHANGES MADE

IN THE CLAIMS

Cancel claims 1-2, 4-18.

19. (New) An assembly structure for a memory device, comprising:

a common substrate having multiple sections;

a first layer of a memory array disposed on a first section of the multiple sections wherein the first layer of the memory array comprises a first plurality of conductor lines;

a second layer of a memory array disposed on a second section of the multiple sections wherein the second layer of the memory array comprises a second plurality of conductor lines;

at least one fold line disposed on the common substrate to define alignment of the memory arrays on the first and second sections;

wherein the sections may be folded on each other at the at least one fold line to form an operable electronic device in the memory device;

wherein at least one of the first and second layers of the memory array comprises semiconductor materials and patterns thereon to form a matrix of memory cells; and

wherein the first and second sections are folded along the at least one fold line so that the layers of the memory array are in contact with each other.

20. (New) The assembly structure recited in claim 19 wherein the first plurality of conductor lines are fabricated with first narrowing cross-section areas at points where the memory cells are capable of a permanent change of state.

21. (New) The assembly structure recited in claim 20, wherein the second plurality of conductor lines includes second narrowing cross-section areas configured to align with the first narrowing cross-section areas.